REMARKS

No claims have been amended. Claims 46-48, 51-56, 58-60, 62-65 and 67-81 are pending in this application. No new matter has been introduced.

Claims 56, 58, 59, 72 and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (U.S. Patent No. 5,963,838)("Yamamoto") and Yamagata et al. (U.S. Patent No. 5,679,475)("Yamagata"). This rejection is respectfully traversed.

The claimed invention relates to semiconductor devices and, in particular, to buried conductors within a substrate. The present invention provides a method of forming a plurality of buried conductors and buried conductor patterns in semiconductor substrates such as monocrystalline silicon substrate, interconnecting those patterns and then filling those empty-spaced patterns with a suitable conducting material.

Yamamoto relates to providing a semiconductor device which allows an easy manufacturing process and a method of manufacturing one that can realize a high integration density. Yamamoto specifically teaches a tunnel 8 formed in a silicon substrate 21 at a position right under the transistor element where a wiring layer 32 is buried. (Abstract; column 19, lines 25-60).

Yamagata relates to a process for preparing a semiconductor substrate 100, providing the use of an epitaxial growth film 102 as an active layer in place of the conventional silicon substrate. Yamagata specifically teaches a method which comprises the steps of porousifying a silicon moncrystalline thin film 102 to epitaxially grow on a surface of the porous layer, oxidizing the surface of the epitaxial growth layer, forming a deposited film 103 on the oxidized surface, thereby obtain a first

substrate, closely contacting the deposited film of the first substrate to a second substrate 110, heat treating the closely contacted substrates and a step of selectively etching the porous layer. (column 4, lines 24-35).

Claim 56 recites a buried conductor pattern within a monocrystalline substrate that comprises "at least one empty spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein." Yamamoto teaches a tunnel 8 which is "formed in the silicon substrate 21 at a position right under the transistor element," (Abstract) and not a buried conductor pattern within a monocrystalline substrate comprising "at least one empty spaced pattern in [the] monocrystalline substrate . . . [and] containing at least one drilled hole therein." Claim 56 further recites "a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate." Yamamoto does not disclose, teach or suggest such a limitation.

The Office Action recommends referring to FIG. 47. In FIG. 47, Yamamoto teaches that the wiring layer 32 is connected to drains 35b and 36b of MOS transistors via a conductive film 37. (col. 19, lines 55-60). The Examiner equates the conductive film 37 of Yamamoto to the conductive path of the present invention. However, the conductive film 37 does not connect the buried conductor pattern with the exterior of the monocrystalline substrate 21 as in the claimed invention. The conductive film 37 in Yamamoto, is an external element to the substrate 21, and thus, cannot connect the "buried conductor pattern with the exterior of [the] monocrystalline substrate." Thus, the claimed conductive path and the conductive film 37 of Yamamoto are not the same. Accordingly, Yamamoto does not teach or suggest all of the limitations of the claim 56 invention.

Nor does Yamamoto in combination with Yamagata teach, suggest or disclose "at least one empty spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein," or "a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate." Yamagata also does not teach or suggest such limitations. Thus, Yamamoto in view of Yamagata fail to teach or suggest the limitations of claim 56.

In addition, there is no motivation for one skilled in the art to combine the teachings of Yamamoto with those of Yamagata. Yamamoto teaches a method of burying layers within a substrate to prevent an increase in the number of wiring layers formed in a substrate. On the other hand, Yamagata teaches a method for preparing a semiconductor substrate, specifically providing the use of an epitaxial growth film as an active layer in place of the conventional silicon substrate. When viewing the two references together, there is no common element in which there respective structures are formed. Accordingly, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Yamagata.

Likewise, independent claims 72 and 75 recite the limitations of "at least one buried conductor pattern provided within a monocrystalline substrate," and "a conductive path extending from said buried conductor pattern." As set forth above, Yamamoto and Yamagata do not disclose, teach or suggest such a buried conductor pattern or conductive path. Hence, Yamamoto and Yamagata fail to teach or suggest the limitations of the claim 72 and 75 inventions.

Whether considered alone or in combination, Yamamoto or Yamagata do not teach, disclose or suggest the claimed inventions of claims 56, 72 and 75. Nor would it have been obvious to one skilled in the art to combine the references to produce the present invention. Further, these limitations have been found patentable under the

cross-referenced U.S. Patent No. 6,383,924. Accordingly, the Office Action has failed to establish a prima facie case of obviousness. Applicants respectfully submit that claims 56, 72 and 75 are allowable. Claims 58 and 59 depend from claim 56 and are allowable along with claim 56. Therefore, for the stated reasons, the withdrawal of the rejection of claims 56, 58, 59, 72 and 75 is respectfully requested.

Claims 46, 51, 52, 54, 55 and 60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata and Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced By Silicon Surface Migration." The rejection is respectfully traversed.

Claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Claim 46 further recites "a conductive path extending from said buried conductor pattern to said devices." Yamamoto fails to teach or suggest "at least one buried conductor pattern provided within a monocrystalline substrate." Moreover, the conductive film 37 of Yamamoto, suggested by the Office Action, does not connect the buried conductor pattern with an interconnect between devices whereas in the claimed invention the conductive path connects "the buried conductor pattern to [the] devices." Nor does Yamagata disclose such a buried conductor pattern and conductive path for the reasons set forth above.

Sato teaches an empty-space formation technique, however Sato does not teach "at least one buried conductor pattern provided within a monocrystalline substrate" or a "conductive path extending from said buried conductor pattern to said devices." Consequently, Yamamoto in view of Yamagata and Sato fail to teach, suggest or disclose the limitations of independent claim 46. For at least these reasons, the Office Action fails to establish a prima facie case of obviousness as to independent claim 46.

Claims 51, 52, 54 and 55 depend from claim 46 and is allowable along with claim 46. Claim 60 depends from claim 56 and should be allowable along with claim 56 based on the reasoning set forth above. Thus, withdrawal of the rejection of claims 46, 51, 52, 54, 55 and 60 is respectfully requested.

Claims 47, 48, and 76-81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata in view of Sato as applied to claims 46, 51, 52, 54, 55 and 60, and in further view of Kenney (U.S. Patent No. 5,583,368). The rejection is respectfully traversed.

Claims 47 and 48 depend from claim 46. As described above, the cited prior art references, whether considered alone or in combination, fail to teach, suggest or disclose all limitations of independent claim 46. Kenney teaches subsurface structures comprising trenches 28 and 34 of varying depths. Thus, Kenney also fails to teach or suggest a buried conductor pattern within a monocrystalline substrate or a "conductive path extending from said buried conductor pattern to said devices." as recited in claim 46.

Claim 76 recites a "first conductive path extending from said first buried conductor pattern and a second conductive path extending from said second buried conductor pattern." As applied to claim 46, the cited references fail to teach or suggest the limitation of a "conductive path extending from . . . [a] buried conductor pattern," as recited in claim 76. The Office Action fails to establish a prima facie case of obviousness as to independent claim 76. Claims 77-81 depend from claim 76 and should be allowable along with claim 76. Accordingly, withdrawal of the rejection of claims 47, 48, and 76-81 are respectfully requested.

Claim 53 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata in view of Sato as applied to claims 46, 51, 52, 54, 55 and 60, and in further view of Witek et al. (U.S. Patent No. 5,291,438). The rejection is respectfully traversed.

Claim 53 which depends from claim 46. As described above, the cited prior art references, whether considered alone or in combination, fail to teach, suggest or disclose all limitations of independent claim 46. Witek teaches germanium as a substrate. Witek does not teach or suggest a buried conductor pattern within a monocrystalline substrate or a "conductive path extending from said buried conductor pattern to said devices," as recited in claim 46. Thus, withdrawal of the rejection of claim 53 is respectfully requested.

Claims 62-64, and 67-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata as applied to claims 56, 58, 59, 72 and 75, and further in view of Tsu et al. (U.S. Patent No. 6,294,420 B1). The rejection is respectfully traversed.

Yamamoto and Yamagata do not teach or suggest the claimed invention for the reasons already stated. Tsu teaches an integrated circuit capacitor and a method of forming a capacitor. Tsu specifically discloses that a capacitor may be used in a DRAM array, and that the memory array may be embedded in a larger integrated circuit device. (Abstract).

Claim 62 recites "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said monocrystalline substrate having at least one hole drilled therein." Claim 62 further recites "a conductive path extending from said conductive structure to said top surface

of said monocrystalline substrate." Yamamoto in view of Yamagata fail to teach or suggest such limitations. When viewed further in view of Tsu, the references still fail to teach or suggest a combination of all of the elements claimed invention. Tsu does not teach, suggest or disclose "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern" or "a conductive path extending from said conductive structure to said top surface of said monocrystalline substrate." Consequently, Applicants respectfully submit that claim 62 is allowable. Claims 63, 64 and 67-71 depend from claim 62 and are allowable along with claim 62.

Claims 73 and 74 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Yamagata in view of Sato, and in further view of Kenney. The rejection is respectfully traversed.

Claims 73 and 74 depend from claim 72. As set forth above, the cited prior art references, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 72. Applicants respectfully submit that claims 73 and 74 are allowable as they depend from claim 72.

Claim 65 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Tsu, and in further view of Sato. The rejection is respectfully traversed.

Claim 65 depends from independent claim 62. As set forth above, the cited prior art references, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 62. Accordingly, withdrawal of the rejection of claim 65 is respectfully requested.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

By_____

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